

Ref. 12588ROUS01U

We claim:

- 5 1. A synchronizer for mapping an electrical digital signal of arbitrary transmission rate for transport over a network characterized by a range of allowable transmission rates, said synchronizer comprising:
- a) an input for receiving the electrical digital signal;
- 10 b) a data recovery unit coupled to said input, said data recovery unit operative to recover from the electrical digital signal a stream of data bits and a first data clock signal indicative of the arbitrary transmission rate;
- 15 c) a clock generator unit coupled to said data recovery unit for receiving the first data clock signal, said clock generator unit operative to process the first data clock signal for generating a second data clock signal indicative of a line transmission rate that falls within the range of allowable transmission rates for the optical network;
- 20 d) a mapping unit in communication with said clock generator unit for receiving the second data clock signal, said mapping unit being operative for mapping the stream of data bits into at least one frame at a line transmission rate indicated by the second data clock signal;
- 25 e) an output for releasing the at least one frame from

Ref. 12588ROUS01U

said synchronizer for transmission over the network.

2. A synchronizer as defined in claim 1, wherein the network is an optical network.
- 5 3. A synchronizer as defined in claim 2, wherein the optical network is an asynchronous optical network.
4. A synchronizer as defined in claim 1, wherein the network is an electrical network.
- 10 5. A synchronizer as defined in claim 4, wherein the electrical network is an asynchronous electrical network.
- 15 6. A synchronizer as defined in claim 1, wherein the at least one frame is characterized by valid timeslots and invalid timeslots, said mapping unit being operative to distribute the bits of the stream of data bits in the valid time slots and providing stuff bits in the invalid time slots.
7. A synchronizer as defined in claim 6, wherein said clock generator unit includes a multiplier.
- 20 8. A synchronizer as defined in claim 7, wherein said clock generator includes one input to receive the first data clock signal and another input to receive a control signal, said multiplier being operative to multiply a frequency of the first data clock signal by a value indicated by the control signal to generate the second data clock signal.
- 25 9. A desynchronizer for reverse mapping a data signal received from a network, the data signal being

Ref. 12588ROUS01U

characterized by a line transmission rate, said desynchronizer comprising:

- a) an input for receiving the data signal from the network;
- 5 b) a clock recovery unit coupled to said input, said clock recovery unit operative to recover from the data signal a data clock signal indicative of the line transmission rate;
- c) a reverse mapping unit operative to extract from
10 the data signal a stream of data bits on a basis of the line transmission rate;
- d) a data transmitter unit coupled to said reverse mapping unit for transmitting the extracted stream of data bits at a selected arbitrary transmission
15 rate;
- e) an output for releasing an electrical signal containing the extracted stream of data bits at the selected arbitrary transmission rate.

10. A method for transmitting an electrical digital signal
20 of arbitrary transmission rate over a network characterized by a range of allowable transmission rates, comprising:

- a) recovering from the electrical digital signal a stream of data bits and a first data clock signal
25 indicative of the arbitrary transmission rate;
- b) processing the first data clock signal for generating a second data clock signal indicative of a line transmission rate that falls within the range of allowable transmission rates for the

Ref. 12588ROUS01U

network;

- c) mapping the stream of data bits into at least one frame at a line transmission rate indicated by the second data clock signal;
- 5 d) releasing an output signal containing the at least one frame.
11. A method as defined in claim 10 wherein the network is an optical network.
12. A method as defined in claim 11, wherein the optical
10 network is an asynchronous optical network.
13. A method as defined in claim 12 wherein the network is an electrical network.
14. A method as defined in claim 13, wherein the electrical network is an asynchronous electrical network.
- 15 15. A method as defined in claim 10, wherein the at least one frame is characterized by valid timeslots and invalid timeslots, the step of mapping the stream of data bits into at least one frame including distributing the bits of the stream of data bits in the valid time
20 slots and providing stuff bits in the invalid time slots.
16. A synchronizer for mapping an electrical digital signal of arbitrary transmission rate for transport over a network characterized by a range of allowable
25 transmission rates, said synchronizer comprising:
- a) input means for receiving the electrical digital signal;

Ref. 12588ROUS01U

- 5 b) data recovery means coupled to said input means,
said data recovery means operative to recover from
the electrical digital signal a stream of data bits
and a first data clock signal indicative of the
arbitrary transmission rate;
- 10 c) clock generator means coupled to said data recovery
means for receiving the first data clock signal,
said clock generator means operative to process the
first data clock signal for generating a second
data clock signal indicative of a line transmission
rate that falls within the range of allowable
transmission rates for the optical network;
- 15 d) mapping means in communication with said clock
generator means for receiving said second data
clock signal, said mapping means being operative
for mapping the stream of data bits into at least
one frame at a line transmission rate indicated by
the second data clock signal;
- 20 e) output means for releasing the at least one frame
from said synchronizer for transmission over the
network.